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SEMICONDUCTOR
TECHNICAL DATA

M68000

ELECTRICAL SPECIFICATIONS

MOTOROLA

MAXIMUM RATINGS

Rating	Symbol	Value				Unit
		MC68000	MC68HC000	MC68008	MC68010	
Supply Voltage	V_{CC}	−0.3 to 7.0	−0.3 to 6.5	−0.3 to 7.0	−0.3 to 7.0	V
Input Voltage	V_{in}	−0.3 to 7.0	−0.3 to 6.5	−0.3 to 7.0	−0.3 to 7.0	V
Maximum Operating Temperature Range MC68000C	T_A	T_L to T_H 0 to 70 −40 to 85	T_L to T_H 0 to 70 —	T_L to T_H 0 to 70 −40 to 85	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature	T_{stg}	−55 to 150	−55 to 150	−55 to 150	−55 to 150	°C

THERMAL CHARACTERISTICS

The following thermal characteristics apply to the MC68000, MC68HC000, MC68008 and the MC68010.

Characteristic	Symbol	Value	Symbol	Value	Rating
Thermal Resistance —	θ_{JA}		θ_{JC}		°C/W
Ceramic, Type L/LC		30		15*	
Ceramic, Type R/RC		33		15	
Plastic, Type P		30		15*	
Plastic, Type FN		45*		25*	

*Estimated

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

POWER CONSIDERATIONS

The average die-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The curve shown in Figure 1 gives the graphic solution to the above equations for the specified power dissipation of 1.5 watts over the ambient temperature range of −55°C to 125°C using a maximum θ_{JA} of 45°C/W. Ambient temperature is that of the still air surrounding the device. Lower values of θ_{JA} cause the curve to shift downward slightly; for instance, for θ_{JA} of 40°/W, the curve is just below 1.4 watts at 25°C.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient air (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

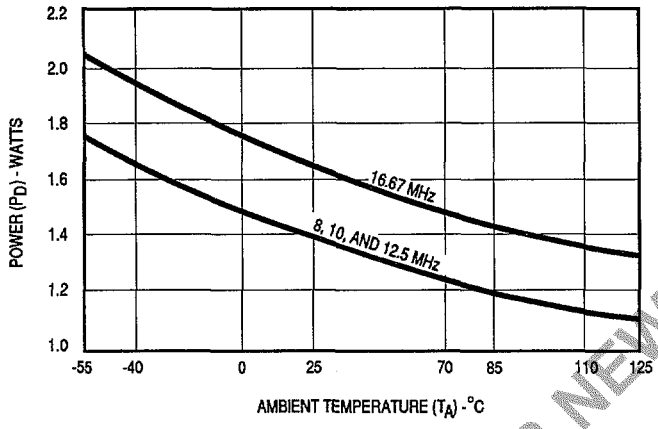


Figure 1. MC68000 Power Dissipation (P_D) vs Ambient Temperature (T_A)

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) results in a lower semiconductor junction temperature.

Table 1 summarizes maximum power dissipation and average junction temperature for the curve drawn in Figure 1, using the minimum and maximum values of ambient temperature for different packages and substituting θ_{JC} for θ_{JA} (assuming good thermal management). Table 2 provides the maximum power dissipation and average junction temperature assuming that no thermal management is applied (i.e., still air).

NOTE

Since the power dissipation curve shown in Figure 1 is negatively sloped, power dissipation declines as ambient temperature increases. Therefore, maximum power dissipation occurs at the lowest rated ambient temperature, but the highest average junction temperature occurs at the maximum ambient temperature where *power dissipation is lowest.*

Values for thermal resistance presented in this manual, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XXX Microcomponent Devices", and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

Table 1. Power Dissipation and Junction Temperature vs Temperature ($\theta_{JC} = \theta_{JA}$)

Package	T_A Range	θ_{JC} (°C/W)	P_D (W) @ T_A Min.	T_J (°C) @ T_A Min.	P_D (W) @ T_A Max.	T_J (°C) @ T_A Max.
MC68000						
L/LC	0°C to 70°C −40°C to 85°C 0°C to 85°C	15 15 15	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
P	0°C to 70°C	15	1.5	23	1.2	88
R/RC	0°C to 70°C −40°C to 85°C 0°C to 85°C	15 15 15	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
FN	0°C to 70°C	25	1.5	38	1.2	101
MC68008						
LC	0°C to 70°C −40°C to 85°C 0°C to 85°C	15 15 15	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
P	0°C to 70°C	20	1.5	30	1.2	95
FN	0°C to 70°C	30	1.5	45	1.3	108
MC68010						
L/LC	0°C to 70°C −40°C to +85°C 0°C to 85°C	15 15 15	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
P	0°C to 70°C	15	1.5	23	1.2	88
R/RC	0°C to 70°C −40°C to +85°C 0°C to 85°C	15 15 15	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
FN	0°C to 70°C	25	1.5	38	1.2	101

NOTE: Table does not include values for the MC68000 12F.

Table 2. MC68000 Power Dissipation and Junction Temperature vs Temperature ($\theta_{JC} \neq \theta_{JA}$)

Package	T_A Range	θ_{JA} (°C/W)	P_D (W) @ T_A Min.	T_J (°C) @ T_A Min.	P_D (W) @ T_A Max.	T_J (°C) @ T_A Max.
MC68000						
L/LC	0°C to 70°C −40°C to 85°C 0°C to 85°C	30 30 30	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
P	0°C to 70°C	30	1.5	23	1.2	88
R/RC	0°C to 70°C −40°C to 85°C 0°C to 85°C	33 33 33	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
FN	0°C to 70°C	40	1.5	38	1.2	101
MC68008						
LC	0°C to 70°C −40°C to 85°C 0°C to 85°C	40 40 40	1.5 1.7 1.5	60 −27 60	1.2 1.2 1.2	121 134 134
P	0°C to 70°C	40	1.5	60	1.2	121
FN	0°C to 70°C	50	1.5	75	1.3	134
MC68010						
L/LC	0°C to 70°C −40°C to +85°C 0°C to 85°C	30 30 30	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
P	0°C to 70°C	30	1.5	23	1.2	88
R/RC	0°C to 70°C −40°C to +85°C 0°C to 85°C	33 33 33	1.5 1.7 1.5	23 −14 23	1.2 1.2 1.2	88 103 103
FN	0°C to 70°C	40	1.5	38	1.2	101

NOTE: Table does not include values for the MC68000 12F.

CMOS CONSIDERATIONS

The MC68HC000, with its significantly lower power consumption, has other considerations. The CMOS cell is basically composed of two complementary transistors (a P channel and an N channel), and only one transistor is turned on while the cell is in the steady state. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus, the overall result is extremely low power consumption because no power is lost through the active P-channel transistor. Also, since only one transistor is turned on during the steady state, power consumption is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become latched in a mode that may result in excessive current drain and eventual destruction of the device. Although the MC68HC000 is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltage specification is not exceeded. Some systems may require that the CMOS circuitry be isolated from voltage transients; others may require no additional circuitry.

The MC68HC000, implemented in CMOS, is applicable to designs to which the following considerations are relevant:

1. The MC68HC000 completely satisfies the input/output drive requirements of CMOS logic devices.

2. The HCMOS MC68HC000 provides an order of magnitude reduction in power dissipation when compared to the HMOS MC68000. However, the MC68HC000 does not offer a "power-down" mode. The minimum operating frequency of the MC68HC000 is 4 MHz.

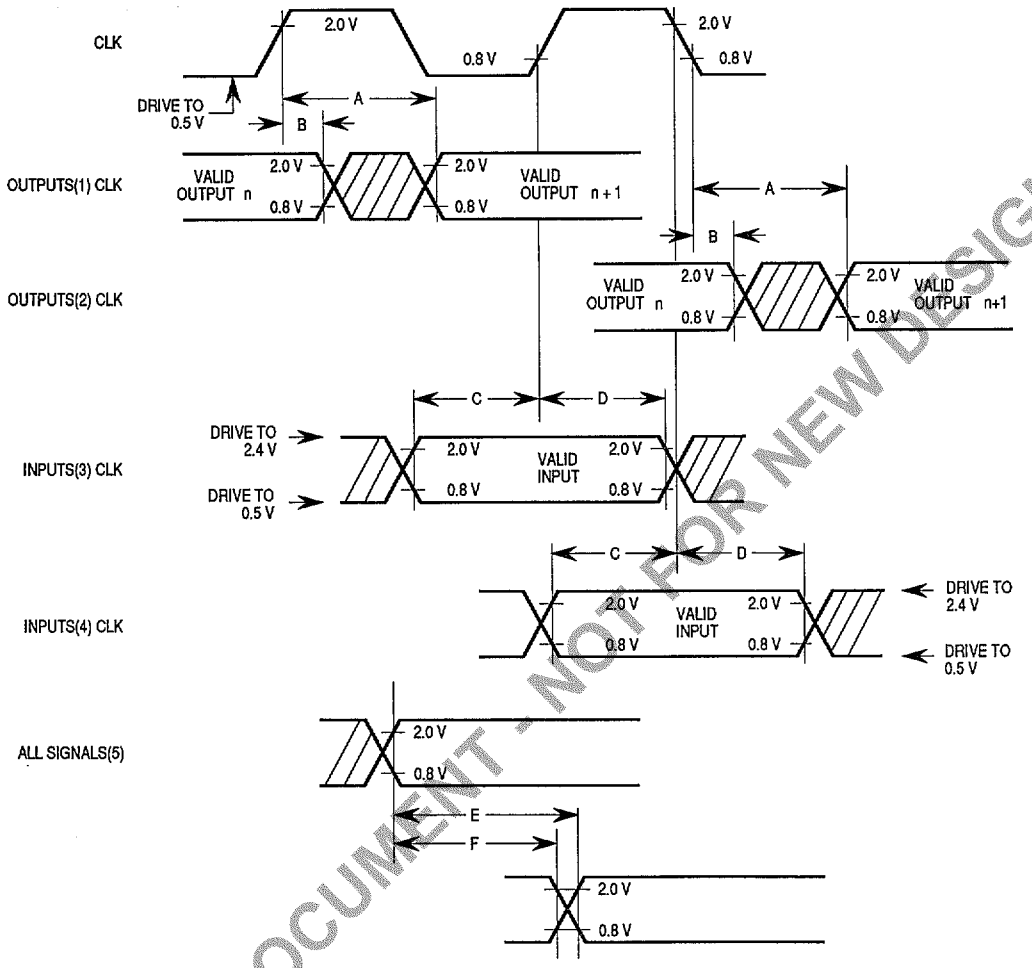
AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 2. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in Figure 2. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown in Figure 2. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications is also shown.

NOTE

The testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 2. Drive Levels and Test Points for AC Specifications

DC ELECTRICAL CHARACTERISTICS (MC68000, MC68008, MC68010)

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND − 0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{VPA}$ $\overline{HALT}$, $\overline{RESET}$	I_{IN}	— —	2.5 20	μA
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A1-A23, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	—	20	μA
Output High Voltage (I_{OH} = −400 μA) (I_{OH} = −400 μA)	E* E, $\overline{AS}$, A1-A23, $\overline{BG}$, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	V_{CC} − 0.75 2.4	— 2.4	V
Output Low Voltage (I_{OL} = 1.6 mA) (I_{OL} = 3.2 mA) (I_{OL} = 5.0 mA) (I_{OL} = 5.3 mA)	 $\overline{HALT}$ A1-A23, $\overline{BG}$, FC0-FC2 $\overline{RESET}$ E, $\overline{AS}$, D0-D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OL}	 — — — —	 0.5 0.5 0.5 0.5	V
Power Dissipation		P_D***	—	—	W
Capacitance (V_{in} = 0 V, T_A = 25°C, Frequency = 1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$ All Others	C_L	— —	70 130	pF

*With external pullup resistor of 1.1 KΩ.
**Capacitance is periodically sampled rather than 100% tested.
***During normal operation instantaneous V_{CC} current requirements may be as high as 1.5 A.

DC ELECTRICAL CHARACTERISTICS (MC68HC000)

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND – 0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{VPA}$, $\overline{HALT}$, $\overline{RESET}$	I_{in}	— —	2.5 20	μA
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A1–A23, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	—	20	μA
Output High Voltage (I_{OH} = –400 μA)	E, $\overline{AS}$, A1-A23, $\overline{BG}$, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	V_{CC} – 0.75	—	V
Output Low Voltage (I_{OL} = 1.6 mA) (I_{OL} = 3.2 mA) (I_{OL} = 5.0 mA) (I_{OL} = 5.3 mA)	 $\overline{HALT}$ A1-A23, $\overline{BG}$, FC0-FC2 $\overline{RESET}$ E, $\overline{AS}$, D0-D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OL}	 — — — —	 0.5 0.5 0.5 0.5	V
Current Dissipation*	f = 8 MHz f = 10 MHz f = 12.5 MHz f = 16.67 MHz	I_D	— — — —	25 30 35 50	mA
Power Dissipation	f = 8 MHz f = 10 MHz f = 12.5 MHz	P_D	— — —	0.13 0.16 0.19 0.26	W
Capacitance (V_{in} = 0 V, T_A = 25°C, Frequency = 1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$ All Others	C_L	— —	70 130	pF

*Currents listed are with no loading.

**Capacitance is periodically sampled rather than 100% tested.

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (see Figure 3)

Num.	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz '12F'		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of Operation	4.0	8.0	4.0	10.0	4.0	12.5	8.0	16.7	8.0	16.7	MHz
1	Cycle Time	125	250	100	250	80	250	60	125	60	125	ns
2,3	Clock Pulse Width (Measured from 1.5 V to 1.5 V for 12F)	55 55	125 125	45 45	125 125	35 35	125 125	27 27	62.5 62.5	27 27	62.5 62.5	ns
4,5	Clock Rise and Fall Times	— —	10 10	— —	10 10	— —	5 5	— —	5 5	— —	5 5	ns

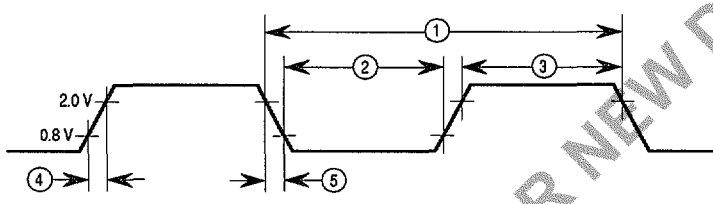
*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68HC000 and are valid only for product bearing date codes of 8827 and later.

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (MC68008)

(see Figure 3)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		Unit
			Min	Max	Min	Max	
	Frequency of Operation	f	2.0	8.0	2.0	10.0	MHz
1	Clock Period	t_{cyc}	125	500	100	500	ns
2,3	Clock Pulse Width	t_{CL}, t_{CH}	55	250	45	250	ns
4,5	Clock Rise and Fall Times	t_{Cr}, t_{Cf}	—	10	—	10	ns

*These specifications represent an improvement over previously published specifications for the 8- and 10-MHz MC68008 and are valid only for product bearing date codes of 8827 and later.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 3. Clock Input Timing Diagram

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 4, 5, 9, 10, and 11)

Num.	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz '12F'		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
6	Clock Low to Address Valid	—	62	—	50	—	50	—	50	—	30	ns
6A	Clock High to FC Valid	—	62	—	50	—	45	—	45	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	80	—	70	—	60	—	50	—	50	ns
8	Clock High to Address, FC Invalid (Minimum)	0	—	0	—	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	3	60	3	50	3	40	3	40	3	30	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	30	—	20	—	15	—	15	—	15	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	90	—	70	—	60	—	30	—	45	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	—	62	—	50	—	40	—	40	3	30	ns
13[2]	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	40	—	30	—	20	—	10	—	15	—	ns
14[2]	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	270	—	195	—	160	—	120	—	120	—	ns
14A	$\overline{DS}$ Width Asserted (Write)	140	—	95	—	80	—	60	—	60	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	150	—	105	—	65	—	60	—	60	—	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES
(Continued)

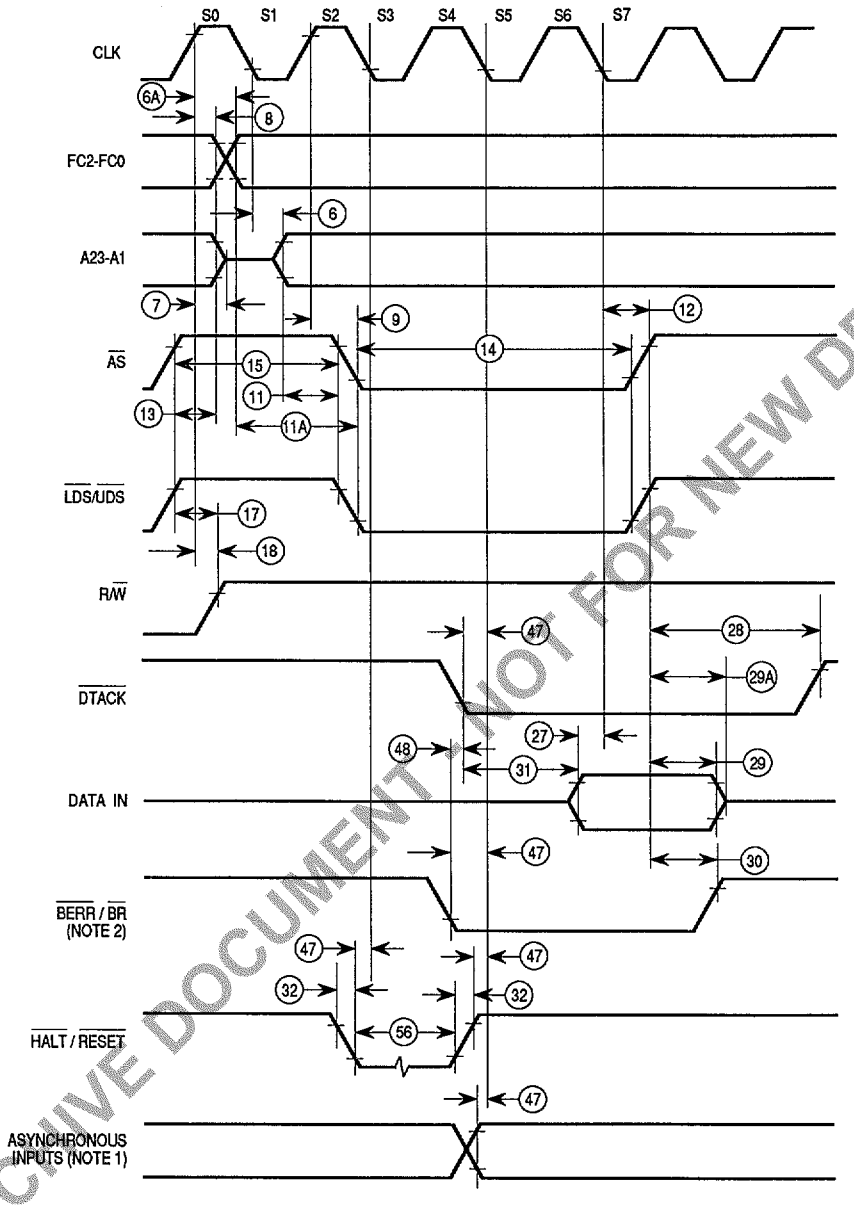
Num.	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz '12F'		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
16	Clock High to Control Bus High Impedance	—	80	—	70	—	60	—	50	—	50	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	40	—	30	—	20	—	10	—	15	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	0	55	0	45	0	40	0	40	0	30	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	0	55	0	45	0	40	0	40	0	30	ns
20A[2,6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Valid (Write)	—	10	—	10	—	10	—	10	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	20	—	0	—	0	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	60	—	50	—	30	—	20	—	30	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	80	—	50	—	30	—	20	—	30	—	ns
23	Clock Low to Data-Out Valid (Write)	—	62	—	50	—	50	—	50	—	30	ns
25[2]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid (Write)	40[10]	—	30	—	20	—	15	—	15	—	ns
26[2]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	40	—	30	—	20	—	15	—	15	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time on Read)	10	—	10	—	10	—	7	—	5	—	ns
27A[5]	Late $\overline{BERR}$ Asserted to Clock Low (Setup Time)	45	—	45	—	45	—	—	—	—	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	0	240[11]	0	190	0	150	0	110	0	110	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	0	—	0	—	0	—	0	—	0	—	ns
29A	$\overline{AS}$, $\overline{DS}$ Negated to Data-In High Impedance	—	187	—	150	—	120	—	90	—	90	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	0	—	0	—	0	—	0	—	0	—	ns
31[2,5]	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time)	—	90	—	65	—	50	—	40	—	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	0	200	0	200	0	200	0	150	—	150	ns
33	Clock High to $\overline{BG}$ Asserted	—	62	—	50	—	40	—	40	0	30	ns
34	Clock High to $\overline{BG}$ Negated	—	62	—	50	—	40	—	40	0	30	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[8]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	20	1.5 Clks	20	1.5 Clks	20	1.5 Clks	10	1.5 Clks	10	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	—	80	—	70	—	60	—	50	—	50	ns
39	$\overline{BG}$ Width Negated	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
40	Clock Low to $\overline{VMA}$ Asserted	—	70	—	70	—	70	—	50	—	50	ns
41	Clock Low to E Transition	—	55[12]	—	45	—	35	—	35	—	35	ns
42	E Output Rise and Fall Time	—	15	—	15	—	15	—	15	—	15	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	0	120	0	90	0	70	0	50	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	30	—	10	—	10	—	10	—	10	—	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES
(Concluded)

Num.	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz '12F'		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
46	$\overline{BGACK}$ Width Low	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
47[5]	Asynchronous Input Setup Time	10	—	10	—	10	—	10	—	5	—	ns
48[2,3]	$\overline{BERR}$ Asserted to $\overline{DTACK}$ Asserted	20	—	20	—	20	—	10	—	10	—	ns
48[2,3,5]	$\overline{DTACK}$ Asserted to $\overline{BERR}$ Asserted (MC68010 Only)	—	80	—	55	—	35	—	—	—	—	ns
49[9]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	−70	70	−55	55	−45	45	−35	35	−35	35	ns
50	E Width High	450	—	350	—	280	—	220	—	220	—	ns
51	E Width Low	700	—	550	—	440	—	340	—	340	—	ns
53	Data-Out Hold from Clock High	0	—	0	—	0	—	0	—	0	—	ns
54	E Low to Data-Out Invalid	30	—	20	—	15	—	10	—	10	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	30	—	20	—	10	—	0	—	0	—	ns
56[4]	$\overline{HALT}$/$\overline{RESET}$ Pulse Width	10	—	10	—	10	—	10	—	10	—	Clks
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	Clks
58[7]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[7]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	Clks

*These specifications represent improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68HC000 and are valid only for product bearing date codes of 8827 and later.

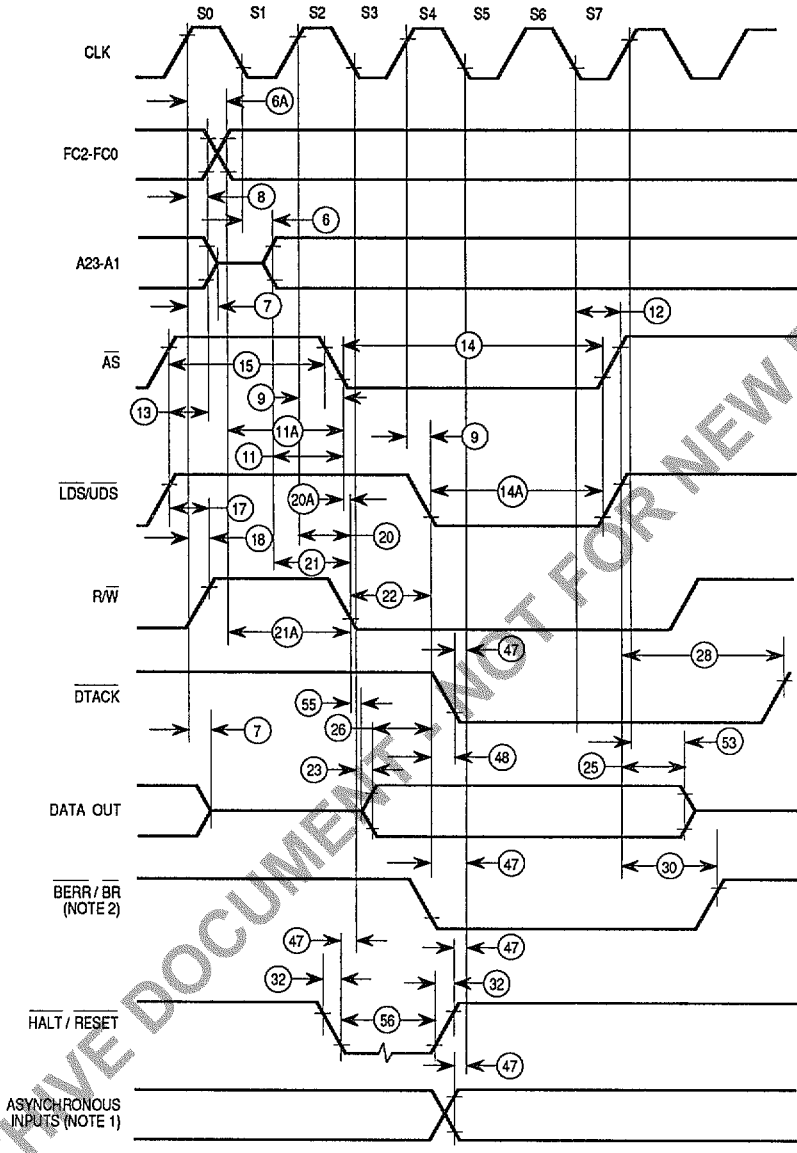
NOTES:
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For power-up, the MC68HC000 must be held in the reset state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be re-asserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and x$\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
10. 245 ns for the MC68008.
11. 50 ns for the MC68008.
12. 50 ns for the MC68008.



NOTES:

1. Setup time for the asynchronous inputs $\overline{IPL2}$-$\overline{IPL0}$ AND $\overline{VPA}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 volt and 2.0 volts.

Figure 4. Read-Cycle Timing Diagram



NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 volt and 2.0 volts.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (specification #20A).

Figure 5. Write-Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — PERIPHERAL CYCLES TO M6800

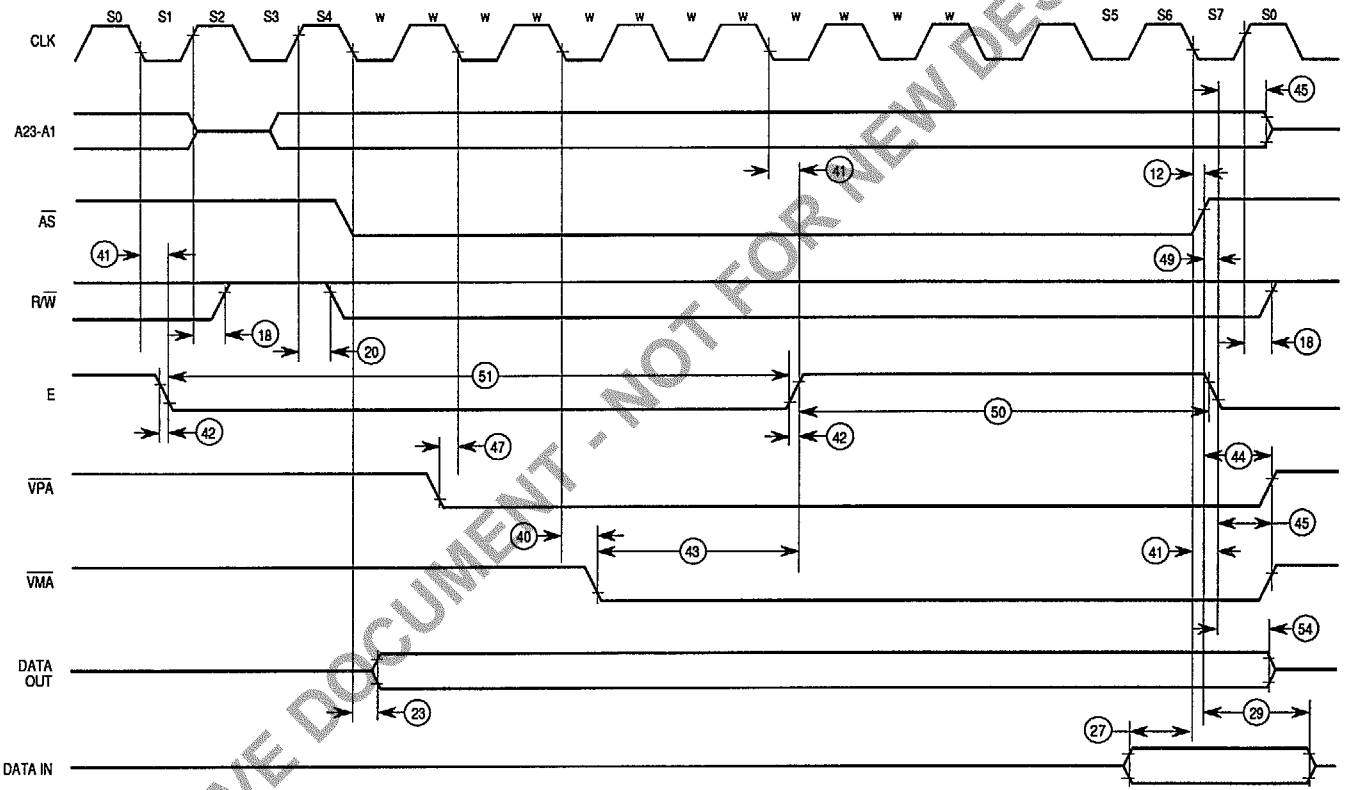
(V_{CC}=5.0 Vdc±5%; GND=0 Vdc; $T_A=T_L$ to T_H; see Figures 6 and 7)

Num.	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz '12F'		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	—	62	—	50	—	40	—	40	3	30	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	0	55	0	45	0	40	0	40	0	30	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	0	55	0	45	0	40	0	40	0	30	ns
23	Clock Low to Data-Out Valid (Write)	—	62	—	50	—	50	—	50	—	30	ns
27	Data-In Valid to Clock Low (Setup Time of Read)	10	—	10	—	10	—	7	—	5	—	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	0	—	0	—	0	—	0	—	0	—	ns
40	Clock Low to $\overline{VMA}$ Asserted	—	70	—	70	—	70	—	50	—	50	ns
41	Clock Low to E Transition	—	55	—	45	—	35	—	35	—	35	ns
42	E Output Rise and Fall Time	—	15	—	15	—	15	—	15	—	15	ns
43	$\overline{VMA}$ Asserted to E High	200	—	150	—	90	—	80	—	80	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	0	120	0	90	0	70	0	50	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	30	—	10	—	10	—	10	—	10	—	ns
47	Asynchronous Input Setup Time	10	—	10	—	10	—	10	—	5[3]	—	ns
49[2]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	−70	70	−55	55	−45	45	−35	35	−35	35	ns
50	E Width High	450	—	350	—	280	—	220	—	220	—	ns
51	E Width Low	700	—	550	—	440	—	340	—	340	—	ns
54	E Low to Data-Out Invalid	30	—	20	—	15	—	10	—	10	—	ns

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68HC000 and are valid only for product bearing date codes of 8827 and later.

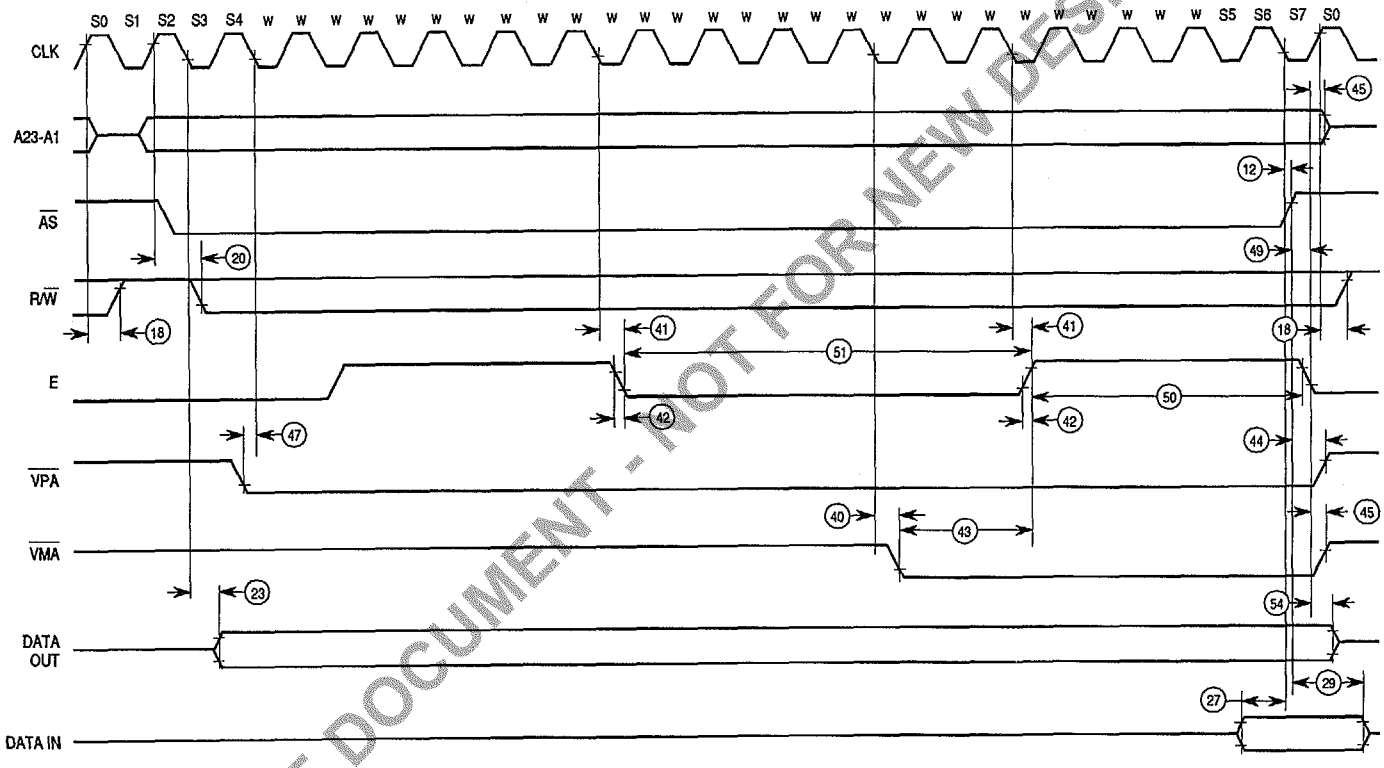
NOTES:

1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. The falling edge of S6 trigger both the negation of the strobes ($\overline{AS}$ and xDS) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
3. 10 ns for MC68000.



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the best case possibly attainable.

Figure 6. Peripheral Timing Diagram (Best Case)



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly attainable.

Figure 7. Peripheral Timing Diagram (Worst Case)

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION

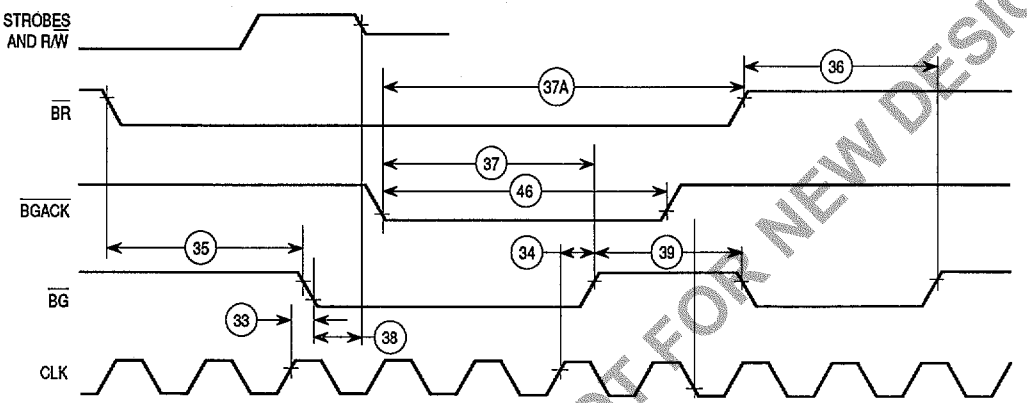
(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 8, 9, 10, and 11)

Num.	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz '12F'		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	80	—	70	—	60	—	50	—	50	ns
16	Clock High to Control Bus High Impedance	—	80	—	70	—	60	—	50	—	50	ns
33	Clock High to $\overline{BG}$ Asserted	—	62	—	50	—	40	—	40	0	30	ns
34	Clock High to $\overline{BG}$ Negated	—	62	—	50	—	40	—	40	0	30	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[1]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[2]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	20	1.5 Clks	20	1.5 Clks	20	1.5 Clks	10	1.5 Clks	10	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	—	80	—	70	—	60	—	50	—	50	ns
39	$\overline{BG}$ Width Negated	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
46	$\overline{BGACK}$ Width Low	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
47	Asynchronous Input Setup Time	10	—	10	—	10	—	10	—	5	—	ns
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	Clks
58[1]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[1]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	Clks

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68HC000 and are valid only for product bearing date codes of 8827 and later.

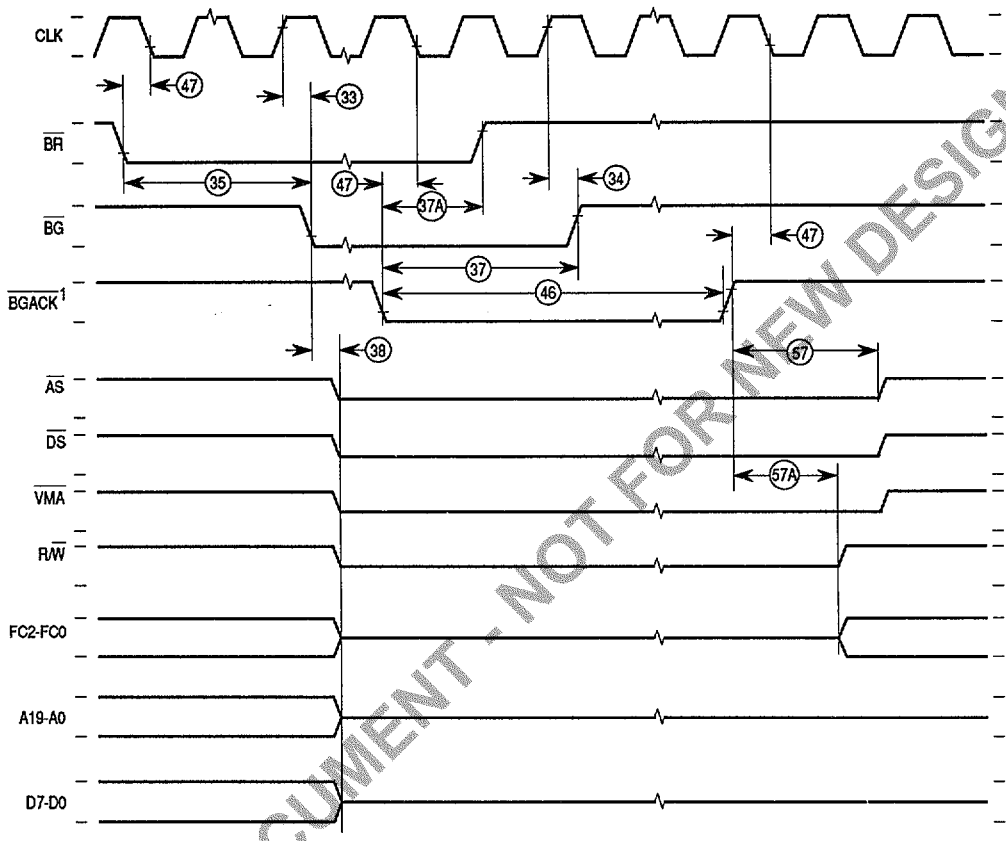
NOTES:

1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
2. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be re-asserted.



NOTE: Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL2-IPL0 and VPA guarantees their recognition at the next falling edge of the clock.

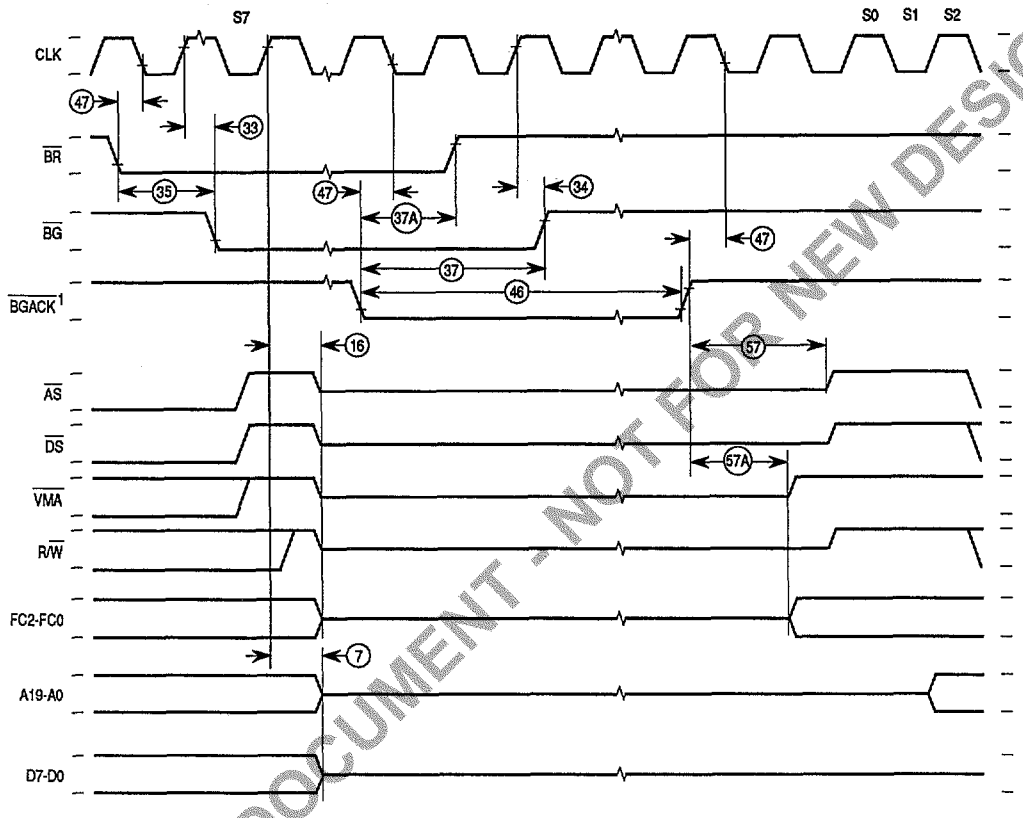
Figure 8. Bus Arbitration Timing



NOTES:

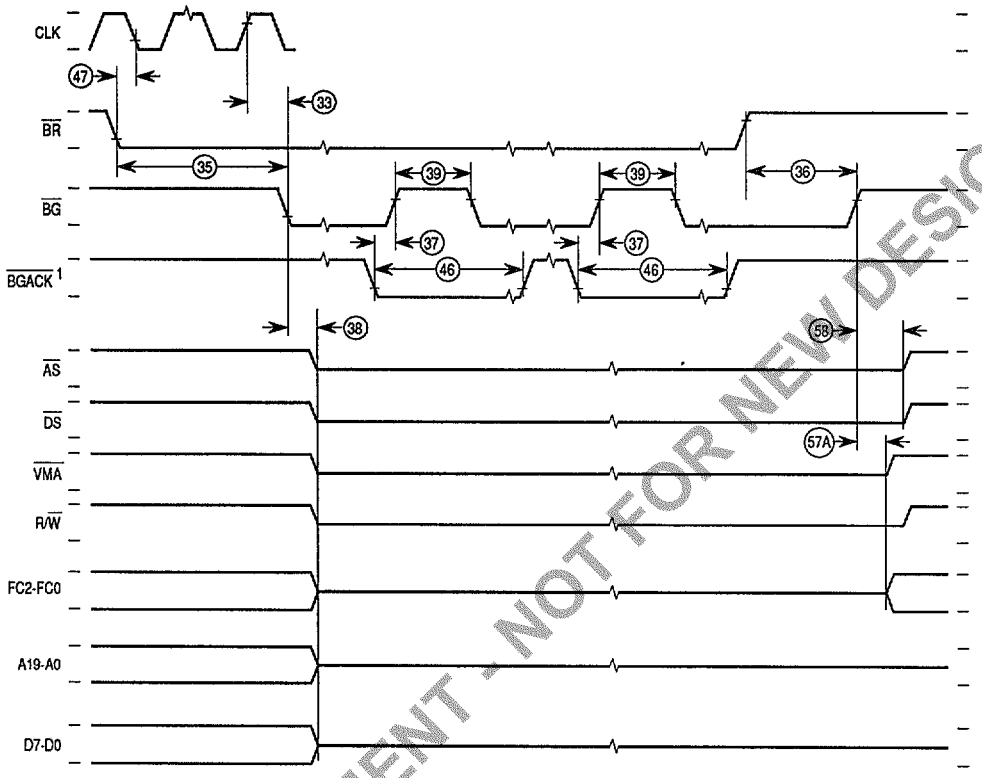
1. Setup time for the asynchronous inputs $\overline{\text{BGACK}}$ and $\overline{\text{BR}}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. Waveform measurements for all inputs and outputs are specified at: logic high 2.0 volts, logic low = 0.8 volt.

Figure 9. Bus Arbitration Timing — Idle Bus Case (52-Pin Version Only for the MC68008)



NOTES:
1. Setup time for the asynchronous inputs $\overline{\text{BGACK}}$ and $\overline{\text{BR}}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. Waveform measurements for all inputs and outputs are specified at: logic high 2.0 volts, logic low = 0.8 volt.

Figure 10. Bus Arbitration Timing — Active Bus Case (52-Pin Version Only for the MC68008)



NOTES:
1. Setup time for the asynchronous inputs BGACK and BR (#47) guarantees their recognition at the next falling edge of the clock.
2. Waveform measurements for all inputs and outputs are specified at: logic high 2.0 volts, logic low = 0.8 volt.

Figure 11. Bus Arbitration Timing — Multiple Bus Request (52-Pin Version Only for the MC68008)

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